**IN THE CLAIMS:**

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claim 1 in accordance with the following:

1. (CURRENTLY AMENDED) A processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal not overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein:

when the first reset signal is input, the first input setting area is initialized after confirmation that the first ~~red~~ flag is cleared and the second initial setting area is initialized after confirmation that the first flag is set and the second flag is cleared, and

when the second reset signal is input, the second initial setting area is initialized after confirmation that the first flag is set and the second flag is cleared without clearing the first flag.

2. (PREVIOUSLY PRESENTED) The processor according to claim 1, further comprising:

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal and which do not overlap with both said first initial setting area and said second initial setting area; and

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed,

wherein:

when any one of the first and second rest signals is input, the third initial setting area is initialized after confirmation that the first and second flags are set and the third flag is cleared, and

when the third reset signal is input, the third setting area is initialized after confirmation that the first and second flags are set and the third flag is cleared without clearing the first and second flags.

3. (PREVIOUSLY PRESENTED) The processor according to claim 2, wherein:

the first initial setting area is formed by a first register group performing communication between the processor and an outside of the processor;

the third initial setting area is formed by a second register group relating to execution of instructions inside the processor; and

the second initial setting area is an area other than both the first register group and the second register group.

4. (PREVIOUSLY PRESENTED) The processor according to claim 2, further comprising:

an n-th initial setting area, where n is an integer having a value equal to or greater than 4, which does not overlap with each initial setting area from the first initial setting area through an (n-1)-th initial setting area and which is initialized based on an input of the first reset signal through an n-th reset signal, different from any of the first through (n-1)-th reset signals; and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein:

when any one of the first, second and third rest signals is input, the n-th initial setting area is initialized after confirmation that the first flag through an (n-1)-th flag are set and the n-th flag is cleared, and

when the n-th reset signal is input, the n-th initial setting area is initialized after confirmation that the first through (n-1)-th flags are set and the n-th flag is cleared without clearing the first through (n-1)-th flags.

5. (PREVIOUSLY PRESENTED) The processor according to claim 1, wherein is an

external input terminal of the processor receives the respective reset signals from the outside.

6. (ORIGINAL) The processor according to claim 1, wherein the respective reset signals are generated within the processor.

7. (PREVIOUSLY PRESENTED) A method of controlling resetting of a processor, the processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal not overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein:

when the first reset signal is input, the first initial setting area is initialized after confirmation that the first flag is cleared and the second initial setting area is initialized after it is confirmed that the first flag is set and the second flag is cleared, and

when the second reset signal is input, the second initial setting area is initialized after confirmation that the first is set and the second flag is cleared without clearing the first flag,

the method comprising:

clearing each of the first and second flags corresponding to each of the first and second signals;

confirming that each of the first and second flags is cleared, and initializing each of the first and second initial setting areas corresponding to each of the first and second flags that is cleared; and

setting each of the first and second flags repeatedly, after completion of initializing each of the first and second initial setting areas, until all of the first and second flags are set.

8. (PREVIOUSLY PRESENTED) A method of controlling resetting of a processor,

the processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal not overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein:

the method comprises:

clearing the first and second flags when the first reset signal is input, and clearing the second flag when the second reset signal is input;

when the first signal is input, initializing the first initial setting area after confirming that the first flag is cleared, and initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared;

when the second rest signal is input, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared, without clearing the first flag; and

setting each of the first and second flags corresponding to each of the first and second initial setting area which initialized.

9. (PREVIOUSLY PRESENTED) A method of controlling resetting of a processor, the processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal not overlapping with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal not overlapping both said first initial setting area and said second initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either of the first and second reset

signals and that is set when initial setting of the second initial setting area has been completed; and

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, wherein:

the method comprises:

clearing the first flag to the third flag when the first reset signal is input, clearing the second and third flags when the second reset signal is input, and clearing the third flag when the third reset signal is input;

when the first signal is input, initializing the first signal initial setting area after confirming that the first flag is cleared, initializing the second signal initial setting area after confirming that the first flag is set and the second flag is cleared, and initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared;

when the second signal is input, initializing the second signal initial setting area after confirming that the first flag is set and the second flag is cleared without clearing the first flag, and initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared;

when the third signal is input, initializing the third initial setting area after confirming that the first and second flags are set and the third flag is cleared without clearing the first and second flags; and

setting each of the first, second, and third flags corresponding to each of the first, second, and third initial setting area which is initialized.

10. (PREVIOUSLY PRESENTED) The method of controlling resetting of a processor according to claim 9, wherein:

the first initial setting area is formed by a first register group performing communication between the processor and an outside of the processor;

the third initial setting area is formed by a second register group relating to the execution of instructions inside the processor; and

the second initial setting area is an area other than both the first register group and the second register group.

11. (PREVIOUSLY PRESENTED) A method of controlling resetting of a processor,

the processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal not overlapping with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal not overlapping both said first initial setting area and said second initial setting area;

an n-th initial setting area, where n is an integer having a value equal to or greater than 4, which do not overlap with each initial setting area, from the first initial setting area through an (n-1)-th initial setting area, and which is initialized based on an input of the first reset signal through an n-th reset signal different from any of the first through (n-1)-th reset signals;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either of the first and second reset signals and that is set when initial setting of the second initial setting area has been completed;

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed; and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein:

the method comprises:

clearing the first flag to the n-th flag when the first reset signal is input, clearing the second flag to the n-th flag when the second reset signal is input, clearing the third flag to n-th flag when the third reset signal is input, and clearing the n-th flag when the n-th reset signal is input;

when the first signal is input, initializing the first signal initial setting area after confirming that the first flag is cleared, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared, initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared, and initializing the n-th initial setting area after confirming that the first flag through an (n-1)-th flag are set and the n-th flag is cleared;

when the second signal is input, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared without clearing the first flag, initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared, and initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared;

when the third signal is input, initializing the third initial setting area after confirming that the first and second flags are set and the third flag is cleared without clearing the first and second flags, and initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared;

when the n-th reset signal is input, initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared without clearing the first through (n-1)-th flags; and

setting each of the first flag to the n-th flag corresponding to each of the first initial setting area to the n-th setting area which is initialized.